REMARKS

The drawings have been objected to for various reasons under 37 C.F.R. § 1.83(a). Claims 1 to 16 are pending in the present application. In an Office Action mailed February 6, 2003, the Examiner rejected claims 1 to 16. Claims 1, 3, 6, 12, 13, 14 and 16 have been amended. New Claim 17 has been added incorporating the limitations of original Claim 16 as they were dependent on Claim 12. Claim 15 has been cancelled. These amendments add no new matter. Upon entry of the above amendments, Applicants respectfully request reconsideration of claims 1 to 14, 16 and 17.

I. Objections to Drawings under 37 C.F.R. § 1.83(a)

The Examiner has objected to the drawings as filed under 37 C.F.R. § 1.83(a). Applicants have amended the Figures to add reference numerals and functional labels as suggested by the Examiner. Support for these amendments may be found in the Figures and the specification which associates the numbering with the functional label added to each box of Figures 1 and 2. These amendments add no new matter.

Particularly, the Examiner objects to the drawings in that the drawings "fail to show 'the at least one input node for the input signal is connected to the at least one evaluation circuit' in claim 3." In support of this position, the Examiner notes that "in figure 3 that is a detailed drawing of claim 1, the input is not connected to the evaluation circuit (40, 41)." Applicants respectfully traverse this objection.

Applicants respectfully submit that Figures 1 to 3 each illustrate an input node (11) connected to at least one evaluation circuit (50, 60) to support the claim 3, as filed. Applicants respectfully submit that the Examiner confused the "feedback circuit (40)" and "feedback capacitor (41)" with the "the evaluation circuits (50, 60)." Applicants have added the numeral "11" to the input node of Figure 3 and has functionally labeled Figures 1 and 2 as suggested by the Examiner. As now numbered and functionally labeled, Applicants submit that Figures 1 to 3 now more clearly show an input node (11) connected to at least one evaluation circuit (50, 60). Therefore, Applicants respectfully submit that a continued objection is improper.

Accordingly, Applicants respectfully request that the Examiner withdraw his objection to the Figures as not supporting Claim 3.

The Examiner also objected to Figures 1 and 3 "because the details in the two drawings are not compatible." In support of this position, the Examiner notes that "in figure 1, the evaluation circuit (50) receives signal (13) and the output signal from the output node (12)" and, "in figure 3, the evaluation circuit (50) receives only one input signal from node (12)." Applicants respectfully traverse this objection.

Applicants respectfully submit that Figures 1 and 3 are compatible. The compatibility of Figures 1 and 3 has been clarified by the labeling of the input node feature in Figure 3 with the numeral "11" in the attached proposed drawings. As now numbered, Applicants submit that Figures 1 to 3 now more clearly show the inputs to evaluation circuit (50). Particularly, both Figures 1 and 3 illustrate an input node (11) to direct an input signal (13) signal to evaluation circuit (50) and an output node (12) to direct the output signal to evaluation circuit (50). Therefore, Applicants respectfully submit that a continued objection to Figures 1 and 3 as incompatible is improper.

Accordingly, Applicants respectfully request that the Examiner withdraw his objection to Figures 1 and 3 as incompatible.

The Examiner objected to Figures 1 and 2 "because functional labels of the boxes are missing." Although Applicants disagree, Figures 1 and 2 have been amended in the proposed amendments attached to this Response to add "functional labels" to the boxes as suggested by the Examiner. Support for these "functional labels" may be found in the numerals associated with the "boxes" and the description of the "boxes" in the specification as filed. Therefore, Applicants respectfully submit that a continued objection to Figures 1 and 2 as unlabeled is improper.

Accordingly, Applicants respectfully request that the Examiner withdraw his objection to Figures 1 and 2 for having unlabeled boxes.

The Examiner further objected to the drawings as not showing every feature of the invention specified in the claims. The Examiner noted that the figures did not illustrate the "at least one input node" and "the input node" of Claim 1; the "at least one control transistor" of Claim 8; and the "one regulating transistor" in Claim 16. Regarding the "at least one input node" of Claim 1, the "at least one input node" for an output signal is generally illustrated in each of Figures 1, 2, and 3 as element "11." Regarding "the input node" of Claim 1, "the input node" of the evaluation circuit is generally illustrated in each of Figures 1, 2 and 3 as element

"51" and/or element "61" depending on the particular embodiment illustrated. Regarding the "at least one control transistor" of Claim 8, the "at least one control transistor" is illustrated in Figure 3 as element "24" and "34" in conjunction with the control transistors' association with sub-driver 20 and sub-driver 30, respectively. Regarding the "at least one regulating transistor" in Claim 15, Applicants have cancelled claim 15 to expedite the prosecution of the present application.

Accordingly, Applicants respectfully request that the Examiner withdraw his objection to Figures 1 and 3 as not showing every feature of the invention specified in the claims.

II. Objections to the Claim 14

The Examiner objected to Claim 14 "because the recitation of 'the drive strength' lacks antecedent basis." Applicants have amended Claim 14 to clarify the antecedent basis.

Accordingly, Applicants respectfully request that the Examiner withdraw his objection to Claim 14 as lacking antecedent basis.

III. Rejections of Claims 1 to 16 under 35 U.S.C. § 112.

The Examiner rejected Claims 1 to 16 under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which the Applicants regard as their invention. Applicants respectfully traverse these rejections.

Regarding Claim 1, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, because the recitation of "the first inverter stage being short-circuited with the input node" is misdescriptive. Although Applicants respectfully disagree with the Examiner, Applicants have amended Claim 1 to clarify this artifact of translation to the English language. As amended, Applicants respectfully submit that Claim 1 is not misdescriptive or indefinite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 1 under 35 U.S.C. § 112, second paragraph, as indefinite.

Regarding Claim 3, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, because the recitation of "at least one input node for the input signal is connected

to the at least one evaluation circuit" is misdescriptive. The Examiner contends that the "evaluation circuit (50) is not connected to any 'at least one input node.'" The Examiner requested that Applicants show in the drawing the "at least one input node and the recited connection. Applicants respectfully disagree with the Examiner and directs the Examiners attention to Figures 1 and 2 illustrating the input node (11) and the requisite connection. Applicants submit that there is no requirement that every Figure illustrates every aspect of a claimed invention. Regardless, Figure 3 as filed illustrates the at least one input node but has not designated the node with the numeral "11." Applicants have provided a proposed amendment to Figure 3 adding the numeral "11" to affirmatively identify the input node (11). Therefore, Applicants respectfully submit that a rejection of Claim 3 as indefinite is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 3 under 35 U.S.C. § 112, second paragraph, as indefinite.

Regarding Claim 6, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, because the recitation of "valuation circuit(s) is/are **at** low impedance" is misdescriptive. Although Applicants respectfully disagree with the Examiner, Applicants have amended Claim 6 designate a "low input impedance" for the input node(s) (51, 61) of the evaluation circuit(s) (50, 60), respectively. In view of the amendment to Claim 6, Applicants respectfully submit that a rejection of Claim 6 as indefinite is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 6 under 35 U.S.C. § 112, second paragraph, as indefinite.

Regarding Claim 12, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, because the recitation of "wherein a low-harmonics current is generated in the driver circuit" is indefinite. The Examiner contends that "it is unclear how a low-harmonics current can be generated by the driver circuit." To answer the Examiner's question, Applicants respectfully submit that a low –harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is in the driver circuit, is a feature which automatically results from the structure of the driver circuit as disclosed in the specification and figures and as claimed in claim 12. Regardless of how the invention accomplishes the claimed result, Applicants respectfully submit that the language of Claim 12 "is clear to a hypothetical person possessing the

ordinary level of skill in the pertinent art" for purposes of 35 U.S.C. §112, second paragraph. See M.P.E.P. 2171. Therefore, Applicants respectfully submit that a rejection of Claim 12 as indefinite is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 12 under 35 U.S.C. § 112, second paragraph, as indefinite.

Regarding Claim 13, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, because the recitation of "a $\sin^2$–shaped current is supplied to the load" is indefinite. The Examiner contends that "it is unclear how the output signal can be the squire of the sine wave." To answer the Examiner's question, Applicants respectfully submit that, in order to obtain the $\sin^2$–shaped current, the two transistors (22, 32) operate as current sources. The embodiment of the pre-driver transistors (22, 32) as current sources and the targeted utilization of the parasitic gat-drain capacitance of the driver transistors (21, 31) enables the charging current profile to achieve the $\sin^2$–shape. Regardless of how the invention accomplishes the claimed result, Applicants respectfully submit that the language of Claim 13 "is clear to a hypothetical person possessing the ordinary level of skill in the pertinent art" for purposes of 35 U.S.C. §112, second paragraph. See M.P.E.P. 2171. Therefore, Applicants respectfully submit that a rejection of Claim 13 as indefinite is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 13 under 35 U.S.C. § 112, second paragraph, as indefinite.

Regarding Claim 12 to 15, the Examiner rejected the claims under 35 U.S.C. § 112, second paragraph, because the claims "are method claims that depend upon an apparatus claim 1." Claim 15 has been cancelled. Although Applicants disagree with the Examiner, Applicants have amended Claims 12 to 14 to direct them to an apparatus claims and to recite functional limitations. Therefore, Applicants submit that a continued rejection of Claims 12 to 14 based on being method claims that depend on apparatus claims is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 12 to 15 under 35 U.S.C. § 112, second paragraph, as indefinite.

Regarding Claim 15, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, as indefinite. Although Applicants respectfully disagree with the Examiner,

Claim 15 has been amended to expedite prosecution. Therefore, Applicants respectfully submit that a rejection of Claim 15 as indefinite is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw Claim 15 from consideration.

Regarding Claim 16, the Examiner rejected the claim under 35 U.S.C. § 112, second paragraph, because Claim 16 simultaneously depends upon Claim 1 directed to an apparatus and Claim 12 directed to a method. Although Applicants respectfully disagree with the Examiner, Claim 16 has been amended to depend solely from Claim 1 and new Claim 17 has been added with the same limitations provided in Claim 16 to depend solely from Claim 12. Further, Claim 12 has been redrafted to direct the claim to an apparatus. In view of these amendments, Applicants respectfully submit that a rejection of Claim 16 as indefinite is inapposite.

Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 16 under 35 U.S.C. § 112, second paragraph, as indefinite.

IV. Rejections of Claims 1 to 3, 6 to 8, and 12 to 16 under 35 U.S.C. § 102(b)

The Examiner rejected Claims 1 to 3, 6 to 8, and 12 to 16 under 35 U.S.C. § 102(b) as anticipated by U.S. Pat. No. 6,163,174 by Friedman et al. Applicants respectfully traverse this rejection of Claims 1 to 3, 6 to 8, and 12 to 16 .

The Examiner contends that Friedman et al. teaches, *inter alia*, "the at least one evaluation circuit having a first inverter stage (I1D) coupled to the input node of the valuation circuit, and also a second inverter stage (I2D), connected in series with the first inverter." Although Applicants respectfully disagree with the Examiner, Claim 1 has been amended for clarification and to expedite the prosecution of the present application.

For a rejection under 35 U.S.C. § 102(b) to be proper, a single cited reference must disclose every element and limitation of the claim to which the reference is applied.[1] Furthermore, these elements "must be arranged as in the claim under review."[2]

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[1] *Structural Rubber Prod. Co. v. Park Rubber Co.*, 749 F.2d 707, 223 USPQ 1264 (Fed. Cir. 1984)

[2] *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)

Applicants submit that, as amended, Claim 1 requires the first inverter comprising a first transistor and a second transistor, the second terminals of which are connected to each other respectively and are connected to the input node of the valuation node. Nowhere does Friedman et al. teach or suggest the first inverter comprising a first transistor and a second transistor, the second terminals of which are connected to each other respectively and are connected to the input node of the valuation node as disclosed and claimed by Applicant. To the contrary, Friedman et al. teaches a digital buffer circuit including an input node and an output node and a back coupling from the output node to a logic NOR gate and a logic NAND gate. No inverter stage is coupled to the input node of an evaluation circuit. Furthermore, the detailed structure of each inverter stage and the connection of the inverter stages with regard to the input node of the evaluation circuit and the input node for the input signal is not taught in Friedman et al. Therefore, a rejection of Claim 1 as anticipated by Friedman et al. is inapposite.

Furthermore, it should be noted that the back coupling according to Friedman et al. serves to accelerate the paths of the driver stages. In Applicants claimed invention, the evaluation circuit serves to measure the edge steepness and to adapt the driver strength in real time or progressively in response to this measurement. Therefore, a rejection of Claim 1 as anticipated by Friedman et al. is inapposite.

Accordingly, Applicants respectfully request that the rejection of Claims 1 to 3, 6 to 8, and 12 to 16 under 35 U.S.C. § 102(b) be withdrawn.

Regarding the particular rejections of each of Claims 2, 3, 6 to 8, and 12 to 16. Each of these claims, directly or indirectly depends from Claim 1. Accordingly, for the reasons stated above regarding the rejection of Claim 1, *inter alia*, the rejections of Claims 2, 3, 6 to 8, and 12 to 16 as anticipated by Friedman et al. are also inapposite.

Accordingly, Applicants respectfully request that the rejections of Claims 2, 3, 6 to 8, and 12 to 16 under 35 U.S.C. § 102(b) be withdrawn.

V. Rejections of Claims 1 to 16 under 35 U.S.C. § 103(a)

The Examiner rejected claims 9 to 13 under 35 U.S.C. § 103(a) as unpatentable over U.S. Pat. No. 6,163,174 by Friedman et al. Applicants respectfully traverse this rejection of Claims 9 to 13.

Regarding Claim 9, the Examiner contends, *inter alia*, that Friedman et al. teaches all the elements of Applicants' claimed invention "except for the limitation that the feedback capacitor is designed as a linear capacitor." Applicants respectfully disagree. In order for a rejection under 35 U.S.C. § 103(b) to be proper, the references or, in the present case, the references and knowledge of one skilled in the art, must teach each and every element of the claimed invention. Furthermore, as the Examiner understands, the Examiner must provide some evidence to properly reject a claim as obvious in view of the ordinary skill in the art. In the present case, the Examiner has provided no evidence, other than the Examiner's own assertion, that a linear capacitor "can be integrated into an existing or base line CMOS fabrication process without adding cost in the form of additional processing."

Regardless, as discussed above regarding the rejection of Claim 1 under 35 U.S.C. § 102(b), nowhere does Friedman et al. teach or suggest the first inverter comprising a first transistor and a second transistor, the second terminals of which are connected to each other respectively and are connected to the input node of the valuation node as disclosed and claimed by Applicant. To the contrary, Friedman et al. teaches a digital buffer circuit including an input node and an output node and a back coupling from the output node to a logic NOR gate and a logic NAND gate. No inverter stage is coupled to the input node of an evaluation circuit. Furthermore, the detailed structure of each inverter stage and the connection of the inverter stages with regard to the input node of the evaluation circuit and the input node for the input signal is not taught in Friedman et al. Claim 9 depends upon Claim 1. Therefore, a rejection of Claim 9 as obvious over Friedman et al. is inapposite.

Accordingly, Applicants respectfully request that the rejection of Claim 9 under 35 U.S.C. § 103(a) be withdrawn.

Regarding Claim 10, the Examiner contends, *inter alia*, that Friedman et al. teaches all the elements of Applicants' claimed invention "except for the limitation that the feedback capacitor is designed as a non-linear capacitor." Applicants respectfully disagree. In order for a rejection under 35 U.S.C. § 103(b) to be proper, the references or, in the present case, the references and knowledge of one skilled in the art, must teach each and every element of the claimed invention. Furthermore, as the Examiner understands, the Examiner must provide some evidence to properly reject a claim as obvious in view of the ordinary skill in the art. In the present case, the Examiner has provided no evidence, other than the Examiner's own assertion, that the use of a non-linear capacitor is obvious.

Regardless, as discussed above regarding the rejection of Claim 1 under 35 U.S.C. § 102(b), nowhere does Friedman et al. teach or suggest the first inverter comprising a first transistor and a second transistor, the second terminals of which are connected to each other respectively and are connected to the input node of the valuation node as disclosed and claimed by Applicant. To the contrary, Friedman et al. teaches a digital buffer circuit including an input node and an output node and a back coupling from the output node to a logic NOR gate and a logic NAND gate. No inverter stage is coupled to the input node of an evaluation circuit. Furthermore, the detailed structure of each inverter stage and the connection of the inverter stages with regard to the input node of the evaluation circuit and the input node for the input signal is not taught in Friedman et al. Claim 10 depends upon Claim 1. Therefore, a rejection of Claim 10 as obvious over Friedman et al. is inapposite.

Accordingly, Applicants respectfully request that the rejection of Claim 10 under 35 U.S.C. § 103(a) be withdrawn.

Regarding Claim 11, the Examiner contends, *inter alia*, that Friedman et al. teaches all the elements of Applicants' claimed invention except for the limitation that "the non-linear capacitors are formed using PMOS and NMOS transistors." Applicants respectfully disagree. In order for a rejection under 35 U.S.C. § 103(b) to be proper, the references or, in the present case, the references and knowledge of one skilled in the art, must teach each and every element of the claimed invention. Furthermore, as the Examiner understands, the Examiner must provide some evidence to properly reject a claim as obvious in view of the ordinary skill in the art. In the present case, the Examiner has provided no evidence, other than the Examiner's own assertion, that the use of non-linear capacitors formed using PMOS and NMOS transistors is obvious.

Regardless, as discussed above regarding the rejection of Claim 1 under 35 U.S.C. § 102(b), nowhere does Friedman et al. teach or suggest the first inverter comprising a first transistor and a second transistor, the second terminals of which are connected to each other respectively and are connected to the input node of the valuation node as disclosed and claimed by Applicant. To the contrary, Friedman et al. teaches a digital buffer circuit including an input node and an output node and a back coupling from the output node to a logic NOR gate and a logic NAND gate. No inverter stage is coupled to the input node of an evaluation circuit. Furthermore, the detailed structure of each inverter stage and the connection of the inverter stages with regard to the input node of the evaluation circuit and

the input node for the input signal is not taught in Friedman et al. Claim 11 depends upon Claim 1. Therefore, a rejection of Claim 11 as obvious over Friedman et al. is inapposite.

Accordingly, Applicants respectfully request that the rejection of Claim 11 under 35 U.S.C. § 103(a) be withdrawn.

Regarding Claims 12 and 13, the Examiner contends, *inter alia*, that Friedman et al. teaches all the elements of Applicant's claimed invention and that "a sine wave input current with low harmonic current-content is inputted to the driver circuit, a sine-wave with low harmonic current is generated and the edge steepness (slew) is independent on the components of the driver circuit." Applicants respectfully disagree. In order for a rejection under 35 U.S.C. § 103(b) to be proper, the references or, in the present case, the references and knowledge of one skilled in the art, must teach each and every element of the claimed invention. Furthermore, as the Examiner understands, the Examiner must come forth with some evidence to properly reject a claim as obvious in view of the ordinary skill in the art.. In the present case, the Examiner has provided no evidence, other than the Examiner's own assertion, regarding the sine wave input.

Regardless, as discussed above regarding the rejection of Claim 1 under 35 U.S.C. § 102(b), nowhere does Friedman et al. teach or suggest the first inverter comprising a first transistor and a second transistor, the second terminals of which are connected to each other respectively and are connected to the input node of the valuation node as disclosed and claimed by Applicant. To the contrary, Friedman et al. teaches a digital buffer circuit including an input node and an output node and a back coupling from the output node to a logic NOR gate and a logic NAND gate. No inverter stage is coupled to the input node of an evaluation circuit. Furthermore, the detailed structure of each inverter stage and the connection of the inverter stages with regard to the input node of the evaluation circuit and the input node for the input signal is not taught in Friedman et al. Claims 12 and 13 depend upon Claim 1. Therefore, a rejection of Claims 12 and 13 as obvious over Friedman et al. is inapposite.

Accordingly, Applicants respectfully request that the rejection of Claim 12 and 13 under 35 U.S.C. § 103(a) be withdrawn.

The Examiner rejected Claims 1 to 16 under 35 U.S.C. § 103(a) as unpatentable over U.S. Pat. No. 6,137,322 over Ten Eyck. Applicants respectfully traverse this rejection of Claims 1 to 16.

Regarding Claim 1, the Examiner contends that Eyck teaches "a driver circuit, having, at least one input node (36) for an input signal and at least one output node (68) for an output signal, having one or more sub-drivers (32, 23, 24, 26, 27, 54, 57, 59) and having a feedback circuit (63, 65, 58), which has one or more evaluation circuits (63, 65), the valuation circuit(s) being connected to the driver(s) and output node (68) of the driver circuit, the at least one evaluation circuit having a first inverter stage (65), coupled to the input node of the valuation circuit, and also a second inverter stage (63), connected in series with the first inverter stage except for the limitation that there is a feedback capacitor connected between the output node of the driver (68) and the input of the first inverter (65)." The Examiner then states that "it is old and well known in the art that the capacitor coupled between the output of a circuit and the input of the other circuit for blocking the DC component of the signal." Accordingly, the Examiner concludes that "it would have been obvious for one skilled in the art to implement a 'feedback capacitor' between the output (68) of the driver and the input of the first inverter (65) for the purpose of blocking the DC component of the output signal for preventing the premature triggering of the input circuit." Applicants respectfully disagree.

At the outset, in order for a rejection under 35 U.S.C. § 103(b) to be proper, the references or, in the present case, the references and knowledge of one skilled in the art, must teach or suggest that the references be combined to produce Applicants' invention. Nowhere does Ten Eyck teach or suggest the problem of providing a driver circuit with which the electromagnetic compatibility of electronic components can be improved nor has the Examiner identified any suggestion for such a combination.

Further, in order for a rejection under 35 U.S.C. § 103(b) to be proper, the references or, in the present case, the references and knowledge of one skilled in the art, must teach each and every element of the claimed invention. Furthermore, as the Examiner understands, the Examiner must provide some evidence to properly reject a claim as obvious in view of the ordinary skill in the art. In the present case, the Examiner has provided no evidence, other than the Examiner's own assertion, that "it is old and well known in the art that the capacitor coupled between the output of a circuit and the input of the other circuit for blocking the DC component of the signal."

Regardless, as amended, Applicants submit that, *inter alia*, the coupling of the feedback signal into the first inverter stage being coupled to the input node of the evaluation circuit and the subsequent second inverter stage is not taught or disclosed by Ten Eyck. Applicants submit that Ten Eyck teaches a controlled feedback of the output signal into the control circuit, wherein the driver transistors are split into a plurality of driver transistors. Furthermore, a transmission gate is provided which is positioned between high sided transistors and low sided transistors. Nowhere does Ten Eyck teach or suggest the coupling of the feedback signal into the first inverter stage being coupled to the input node of the evaluation circuit and the subsequent second inverter stage as claimed by Applicants. Therefore, a rejection of Claim 1 as obvious over Ten Eyck is inapposite. Furthermore, a rejection of Claims 2 to 16 which depend directly or indirectly from Claim 1 is also inapposite for the same reasons as the rejection of Claim 1 is inapposite.

Accordingly, Applicants respectfully request that the rejection of Claim 1 to 16 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of Applicants' remarks, the claims are believed to be in condition for allowance. Reconsideration, withdrawal of the rejections, and passage of the case to issue is respectfully requested.

A fee for an extension of time under 37 C.F.R. § 1.136 has been provided. If there are any additional fees are due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 023732.

Respectfully submitted,

Date: Aug. 6, 2003

By _____

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FIG 1

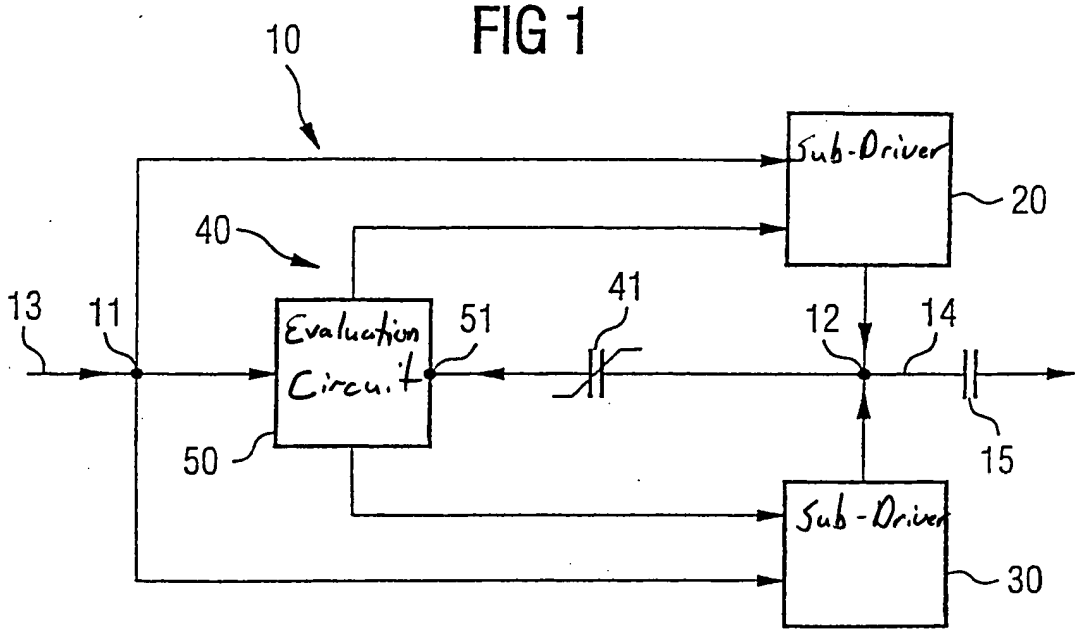

FIG 2

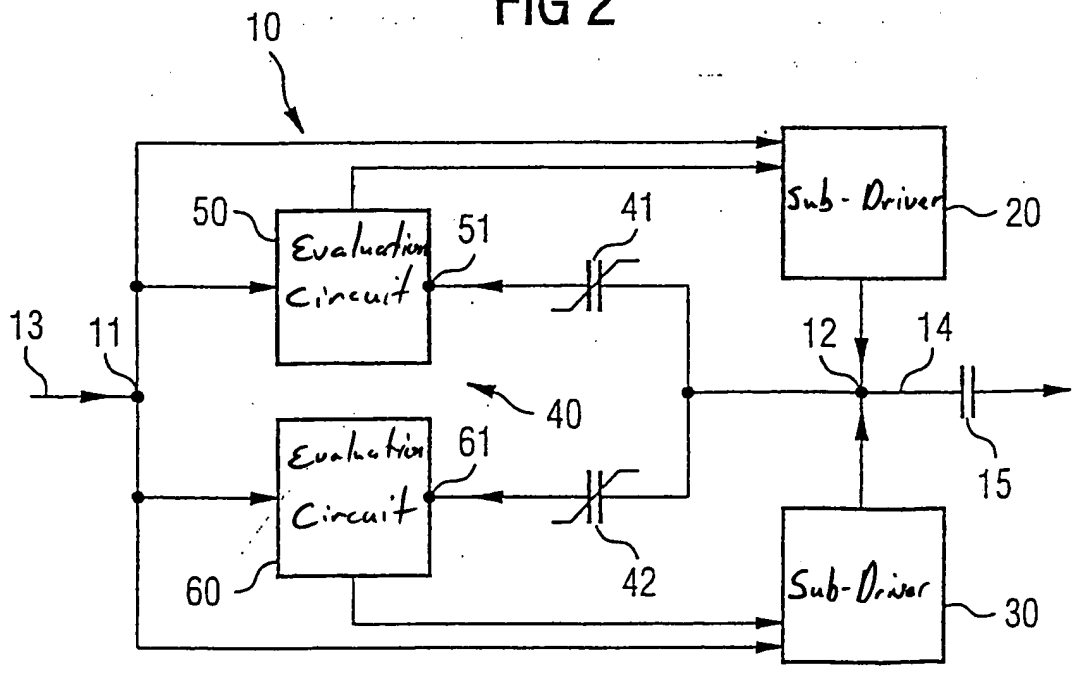

FIG 3